FPGA USE FOR DETECTION AND DIAGNOSIS OF POWER SYSTEMS FAULTS

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Abstract.*High impedance faults occur in power systems because of insulation failure due to increasing in applied electric field. Such unpredictable faults can cause substantial damages if they are not detected precociously and isolated promptly. The main drawback is the difficulty of extracting relevant information on these faults. Indeed, the currents generated in the network are at very low amplitudes and have random frequencies. Many techniques are presently used in power systems diagnosis. Most of them are based on detecting faults by voltages and currents analysis.*

In this paper, a new method of electrical arc faults detection is presented. It is possible by using a Field Programmable Gate Array (FPGA) to create a system which is able to detect the presence of unwanted frequencies in the distribution network. These frequencies are often generated by electrical arc occurrence in the network. The implementation of the system on the network will depend on the ability to test on a real distribution network. In the present case, the tests have been performed on laboratory prototype in order to reduce the risks and costs of a full-scale experiment. Finally, experimental results are provided to validate the performance of the digital implementation.

1. Introduction

The primary purpose of an electrical network is to provide power to consumers. These electrical networks must be protected to ensure the most constant electricity supply.

Currently, to protect distribution networks, several protection devices are installed. These devices react when electrical faults occur. However, some faults such as electrical arcs, especially high impedance faults, cannot be adequately detected by the standard protection devices [1]. These faults can lead to several serious problems [2, 3].

In recent decades, several studies have been conducted to try finding techniques to detect arcing high impedance faults [4]. Several studies have been performed on the harmonic content using the Fast Fourier Transform (FFT) [5, 6]. Other research works have also been based on Kalman filtering and fractal art [7]. However, these studies describe more technical calculations and they have not been tested in all possible cases. Their effectiveness can therefore not be determined.

Artificial Neural Networks [8,9] and Genetic Algorithms [10] have been also proposed by other authors. However, these two techniques have better performance when combined with wavelet transform [11, 12]. Several approaches have been proposed to analyze the wavelet transform.

Several researches were then started to find a system which can recognize an electric fault with high impedance and the electric arc. A few years ago, the realization of an assembly in numerical electronics implied the use of a big number of logical integrated circuits.

The availability of programmable logical circuits such as FPGA (Field Programmable Gate Array) allowed the integration of the numerical circuitry as well as the treatments of the signals in real-time with a great flexibility and a good performance (parallelism of treatment, speed, surface, consumption… etc).

This paper proposes a new method for electrical arc faults detection in a distribution network. It is intended to be a demonstration of how the FPGA is capable of detecting these faults.

2. Experimental setup

Laboratory experiments were performed to detect the high impedance faults in a prototype electrical network. It consists mainly of three sensors of current, signal conditioning circuits (Protection Circuit, Interface Circuit and Digital to Analog Circuit) and Spartran 3E FPGA Board.

The experimental setup is presented in Figure 1.

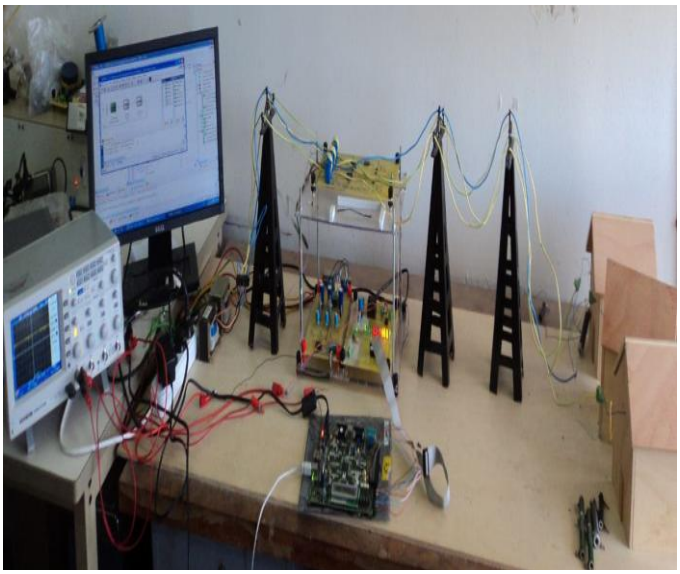

Fig. 1. General view of the experimental setup

The implementation of the experimental device required great attention in order to ensure a good signal processing by the FPGA control module.

The current measurement is provided by Hall effect current sensors, which presents an adequate solution because it provides galvanic insulation between the power circuit and the control circuit.

The protection circuit allows a better conditioning of the signal (offset).

The interface circuit protects the control circuit against occurrence of electrical faults in the power system.

Figure 2 illustrates the functional diagram of the experimental setup.

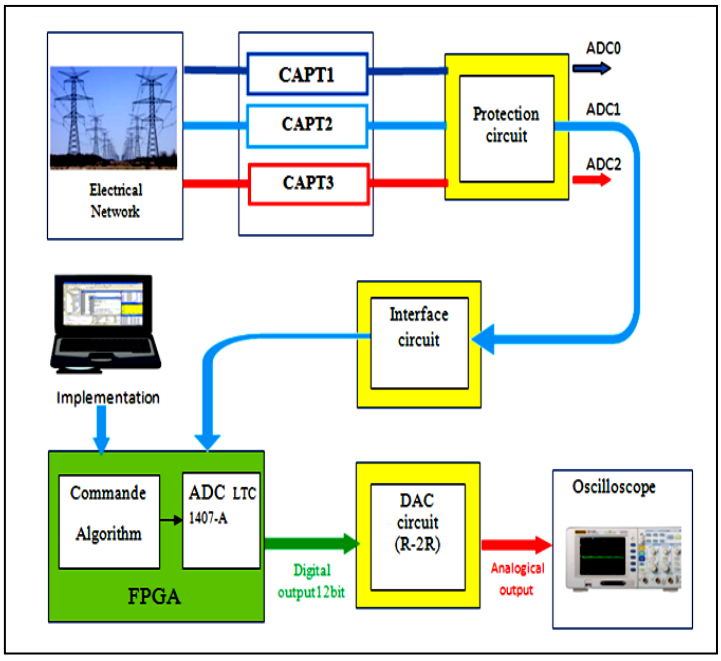

Fig. 2. Synoptic diagram of the experimental setup

3. Description of the experimental procedure

The detection of electrical arcs in distribution networks is provided using a SPARTRAN 3E FPGA board.

An intermediate circuit must be set up between the network and the FPGA to make sure of compatibility between the two systems and the protection of our card of development. After acquisition by the system of measurement, the FPGA card analyzes the current of the phase in the presence of an electric arc fault.

The implemented program in the FPGA is divided into four main parts: data acquisition, analog to digital conversion, FFT and digital to analog conversion.

The following diagram shows the steps of the implemented program:

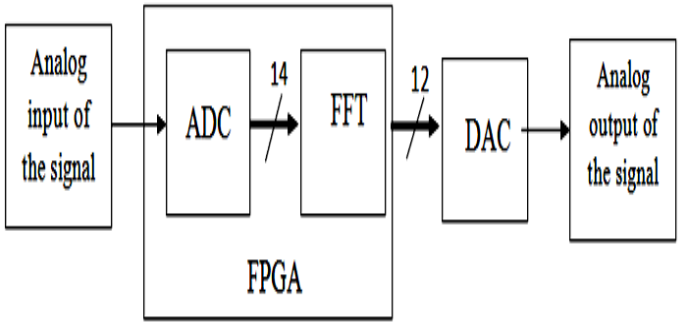

Fig. 3. General flowchart of the implemented program.

Data acquisition: The first step is to measure and convert the currents flowing through the lines of the distribution network into very low voltage. Then, it will be possible to analyze these currents using the FPGA. In most network distribution stations, there is a current transformer already connected to analyze current overloads.

Prior to the analysis of the power distribution network using the FPGA, it is necessary to convert these currents into voltages of amplitude 3V peak-to-peak. The FPGA board used in this work was the Spartan3E Starter kit. Its pin is compatible to an input voltage range of 0 to 3V. An intermediate circuit has been made to adjust the current sensors of the voltages to be compatible with the FPGA.

Analog to Digital Conversion (ADC): The Spartan 3E FPGA board has an analog to digital converter hardware module that allows analog to digital conversion. The digital representation of the sampled analog values is shown as a 14-bit, two's complement binary value by the ADC. The conversion channels are both programmed and controlled by the FPGA through SPI communication protocol. The ADC chip used is LTC1407A.

The value of the digitized data is stored in an array of registers, so that it can be used for further processing.

FFT: To visualize the harmonics of the input signal during the occurrence of an electrical fault in the network, the algorithm of Fast Fourier Transform is used. It is located on the Spartan 3E FPGA card. Then after the processing of the digitized values of the signal with the required functionality, the data is sent to the DAC so as to convert the digitized data into the corresponding analog signal.

Digital to Analog Conversion (DAC): It is to be seen that all the physical signals are analog in nature but their processing obviously happens in the digital domain. So for our application, we have properly designed a digital to analog converter (DAC) which is used to convert the digital voltage value to an analog value. It is based on the principle of the R-2R network.

An R–2R resistor Ladder network is a simple way to perform digital-to-analog conversion, using repetitive arrangements of precise resistor networks in a ladder-like configuration. A string resistor ladder implements the non-repetitive reference network.

This converter generates voltages from 0 to 3Volts output equivalent to the weight of the binary word 12 bits of the input lines (MSB to LSB).

Figure 4 shows the Block diagram of the Digital to Analog Converter.

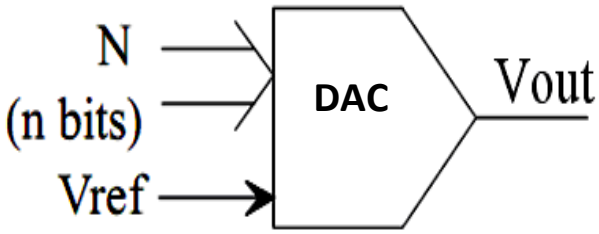

Fig. 4. Block diagram of the DAC.

The Digital to Analog Conversion formula is given below:

$$v_{out} = N.\frac{v_{ref}}{2^{n+1}} \qquad (1)$$

v_{out} : The output voltage.
v_{ref} : The reference voltage.
N : The digital value.
n : Number of bits.

Figure 5 shows the general view of the Digital to Analog Converter.

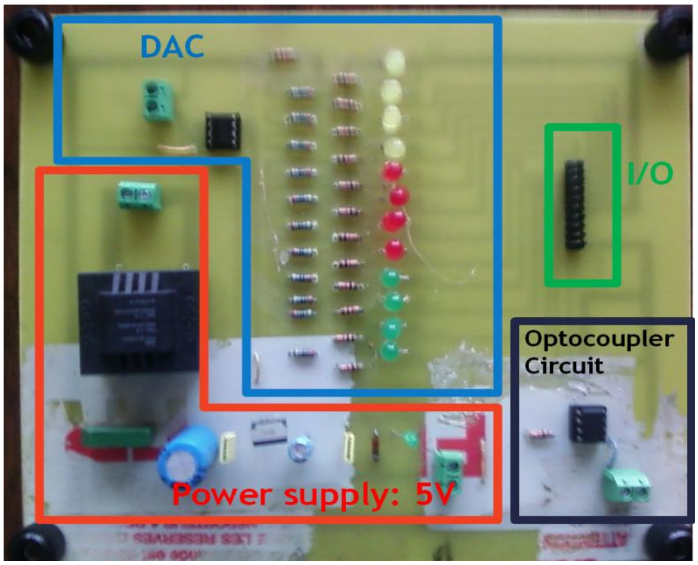

Fig. 5. Picture of the DAC converter.

4. Results and discussion

Several tests were performed on a prototype electrical network designed and realized in laboratory to ensure separate operation of each part of the experimental device.

Figure 6shows the output of the amplifier without any fault and figure 7depicts the FFT of the same signal.

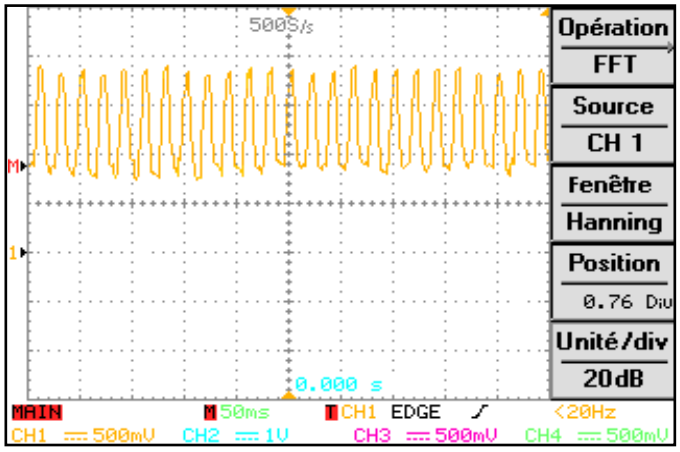

Fig. 6. ADC1 signal without fault.

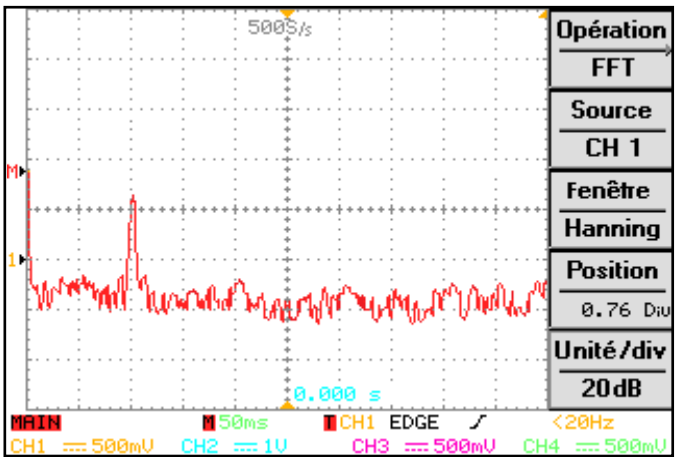

Fig. 7. FFT of ADC1 signal without fault.

On the other hand, when a high impedance fault occurs, the output of the amplifier become clearly different. We simply created an electrical fault in phase 1 by connecting and disconnecting the load, or by putting a wire in the neutral.
Figure 8shows the output of the amplifier with default and figure 9depicts the FFT behavior of the same signal.

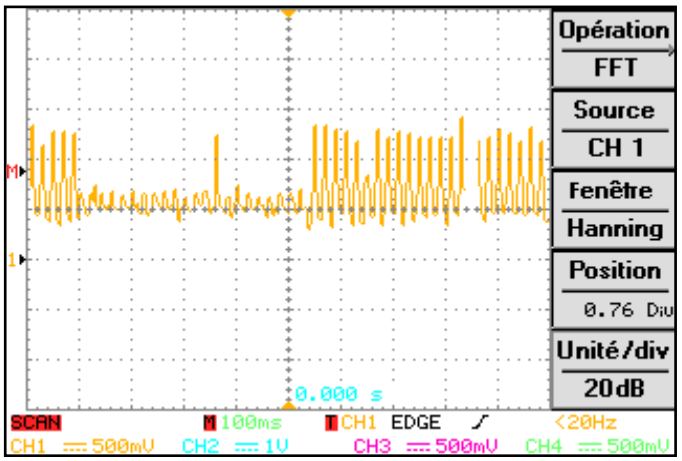

Fig. 8. ADC1 signal with fault.

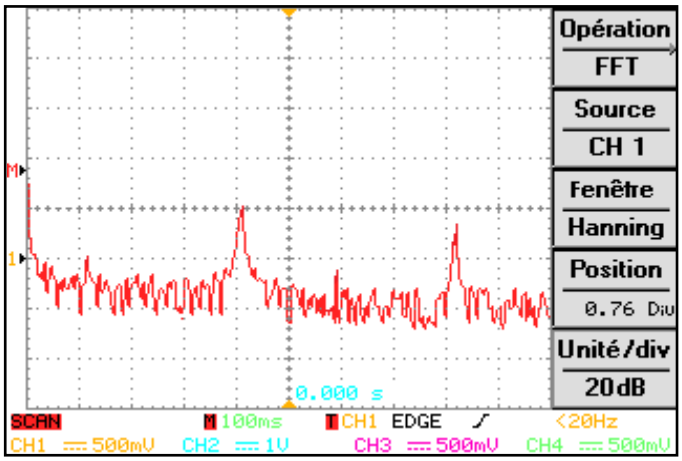

Fig. 9. FFT of ADC1 signal with fault.

The analysis of the results of the entire system on several possible cases has indicated that there are many frequency components at all times. However, when creating electrical faults in high impedance, the harmonics amplitude in the high frequency range increases considerably.

5. Conclusion

The experimental study showed that electric arcs and high impedance faults produce several high and random harmonic frequencies.
The proposed system mainly based on FPGA technology provides a relevant technique for the detection of faults related to electric arcs and high impedance faults.
The realized system is successfully tested on a distribution network designed in laboratory where the FPGA processes the information on the electrical network in real time.

In a next future, a counter will be integrated in the implemented program to calculate the number of harmonics. If the predetermined number is reached in a short time interval, a signal will be sent from the FPGA card to the monitoring device that allows the distribution network opening.

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